REMARKS

I. Status of the claims

Upon entry of the present amendment claims 6 -18 are pending in the present application. Claims 6-13 have been withdrawn from consideration. Claim 14 is the independent claim under consideration.

II. Response to Rejections Under 35 USC § 102 and 103

1. *Rejection Under 35 USC § 102*

Claims 1-5 were rejected under 35 USC § 102(e) as being anticipated by the reference to *Isobe, et al.* (US Patent 6,337,504B1). Claims 1-5 have been canceled, and claims 14-18 are presently under consideration. For the reasons set forth below, it is respectfully asserted that claim 14, and the claims that depend therefrom are allowable over the reference to *Isobe, et al.*

In order to properly establish a prima facie case of anticipation, it is required that ***all*** of the claimed elements be disclosed in the applied art. It follows that if a ***single*** element is neither taught nor suggested in the applied art, a prima facie case of anticipation can be established.

Independent claim 14, recites the limitation that:

"...a thermally diffused second impurity region...extends from a surface of said semiconductor substrate and below said gate electrode."

It is respectfully submitted that at least the recited limitation is not taught in the applied reference to *Isobe, et al.* To this end, the reference to *Isobe, et al.* is drawn to a

semiconductor device that has a lightly doped drain (LDD) layer (field relaxation layer 8) by an ion implantation sequence.

As applicant's disclosure points out, the use of ion implantation for forming the LDD results in its having an impurity distribution that is not gradually lowered from the surface of the device (substrate), but becomes increased at a predetermined depth from the surface and exhibits its maximum level at a predetermined depth and then becomes decreased gradually as the depth from the surface increases. As a result, short channel effects mitigated ineffectively because of the position of the impurity. (Please refer to page 2, lines 7-27 of the application as filed).

In stark contrast, the thermally diffused second impurity region extends from the **surface of the substrate**. Accordingly, the semiconductor device of the invention of claim 14 is more effective at mitigating short channel effects.

Because of the method of forming the LDD regions disclosed, the reference to *Isobe, et al.* necessarily lacks at least a teaching of the recited limitation, it cannot serve to establish a *prima facie* case of anticipation. As such, it is believed that claim 14, and the claims that depend therefrom are allowable over *Isobe, et al.* Allowance is earnestly solicited.

2. *Rejection Under 35 USC § 103*

Claims 1 and 5 were rejected under 35 USC § 103(a) as being unpatentable over *Iguchi, et al.* (US Patent 5,734,185) and *Fang, et al* (US Patent 6,316,323).

For the reasons set forth below, and consistent with those discussed above, newly added claims 14-18 are believed to be allowable over the applied references.

The establishment of a *prima facie* case of obviousness required that *all* of the elements be found in the prior art. As such, it follows that if a single element is not found in the prior art, a proper *prima facie* case of obviousness cannot be established. Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion or motivation to do so found in the references relied upon. However, hindsight in never an appropriate motivation for combining references and/or the requisite knowledge available to one having ordinary skill in the art. To this end, relying upon hindsight knowledge of applicants' disclosure when the prior art does not teach nor suggest such knowledge results in the use of the invention as a template for its own reconstruction. This is wholly improper in the determination of patentability.

As described above, independent claim 14 recites that the thermally diffused second impurity regions extend from the surface of the semiconductor substrate. Moreover, as discussed above, ion implantation results in the impurity region's having its maximum value at a certain depth from the surface, which is disadvantageous from at least the perspective of mitigating short channel affects in devices.

The references to *Iguchi, et al.* and *Fang, et al* both teach the fabrication of impurity regions by ion implantation, and therefore, these regions cannot result in the thermally diffused regions extending from the surface as is claimed.

Accordingly, neither the reference to *Iguchi, et al.* nor the reference to *Fang, et al.* teach the limitation set forth in independent claim 14. As such, because the applied art lacks the teaching of at least one of the elements of independent claim 14; and without

passing whether these references are properly combined, these references cannot serve to establish a *prima facie* case of obviousness. Therefore, claim 14 and the claims that depend therefrom are believed to be allowable over the applied art.

Conclusion

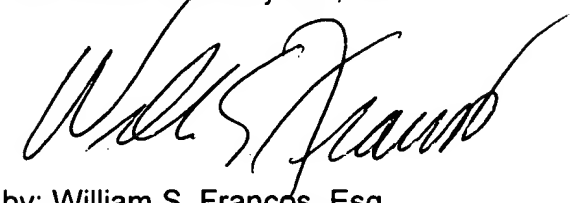
Withdrawal of all objections and rejections is respectfully requested. For at least the reasons set forth above claims 14-18 are believed to be allowable over the applied art. Allowance thereof is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted on behalf of:

Oki Electric Industry Co., Ltd.



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